Claims

1. A first sense amp circuit comprising:

a pre-charge circuit coupled to an input data line, the input data line being coupled to an input of a first inverter;

a keeper circuit coupled in parallel with the first inverter;

a select device coupled to a discharge path of the first inverter; and

a driver device coupled in parallel to an output data line of the first inverter.

2. The circuit of claim 1, further comprising a half latch circuit coupled to the input data line.

3. The circuit of claim 2, wherein the half latch circuit includes a first input and a second input, the first input coupled to an inverse of a pre-charge control signal, the second input coupled to the output of the first inverter.

4. The circuit of claim 1, wherein the select device includes a select control signal coupled to a control input of the select device.

5. The circuit of claim 1, wherein the select device controls the discharging of the first inverter.

6. The circuit of claim 1, wherein the driver device includes a NAND gate and a second inverter, the NAND gate having a first input coupled to a select control signal and a second input coupled to an output of the second inverter, the second inverter having an input coupled to the output of the first inverter, the output of the NAND gate being coupled to the output of the first inverter.

7. The circuit of claim 1, wherein the driver device is not in series with a data signal path through the first inverter.

8. The circuit of claim 1, further comprising:

a second NAND gate having a first input coupled to an output of the first inverter;

a second sense amp circuit having an output coupled to a first input of the second NAND gate;

9. The circuit of claim 8, wherein a total delay through each of the first sense amp circuit and the second sense amp circuit and the second NAND is substantially equal to a two-gate delay.

10. The sense amp circuit of claim 1, wherein the first inverter includes a skewed inverter.

11. A method of detecting a data signal level comprising:

pre-charging an input data line of a first inverter;

receiving a data signal on the input data line sufficient to cause the first inverter to switch;

outputting an output data signal level in less than a two-gate delay;

disabling the pre-charging the input data line of the first inverter; and

resetting the output data signal level when a control signal is received.

12. The method of claim 11, wherein resetting the output data signal level includes applying a predetermined voltage level to the input data line of the first inverter.

13. The method of claim 11, wherein resetting the output data signal level includes applying a predetermined voltage level to an output of the first inverter when the select signal is received.

14. The method of claim 11, wherein resetting the output data signal level includes discharging the first inverter when the select signal is received.

15. The method of claim 11, further comprising driving the output data signal.

16. The method of claim 15, wherein driving the output data signal includes applying a predetermined voltage level to an output of the first inverter.

17. The method of claim 11, further comprising:

coupling an output of the first inverter to a first input of a second NAND gate; and

coupling an output of the second inverter to a second input of the second NAND gate;

18. The method of claim 17, wherein a total delay through each of the first sense amp circuit and the second sense amp circuit and the second NAND is substantially equal to a two-gate delay.

19. The method of claim 11, wherein the first inverter includes a skewed inverter.

20. A circuit comprising:

a first sense amp circuit having a delay substantially equal to a one-gate delay;

a second sense amp circuit having a delay substantially equal to a one-gate delay;

a multiplexer device having a first input coupled to an output of the first sense amp circuit and a second input coupled to an output of the second sense amp circuit; and

a selection device coupled to a selection control of each of the first sense amp circuit and the second sense amp circuit.